5953263

FIG_1

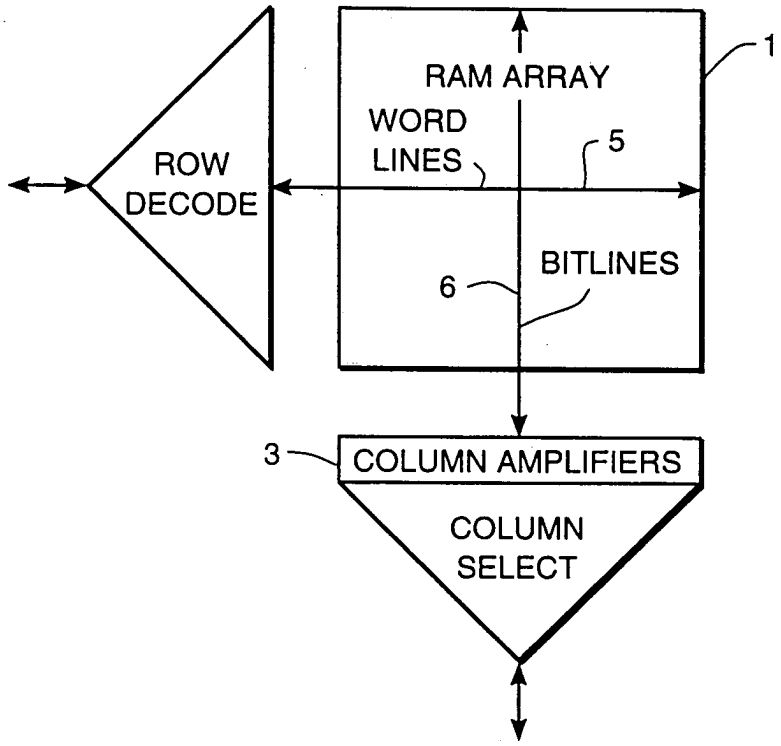


FIG_2

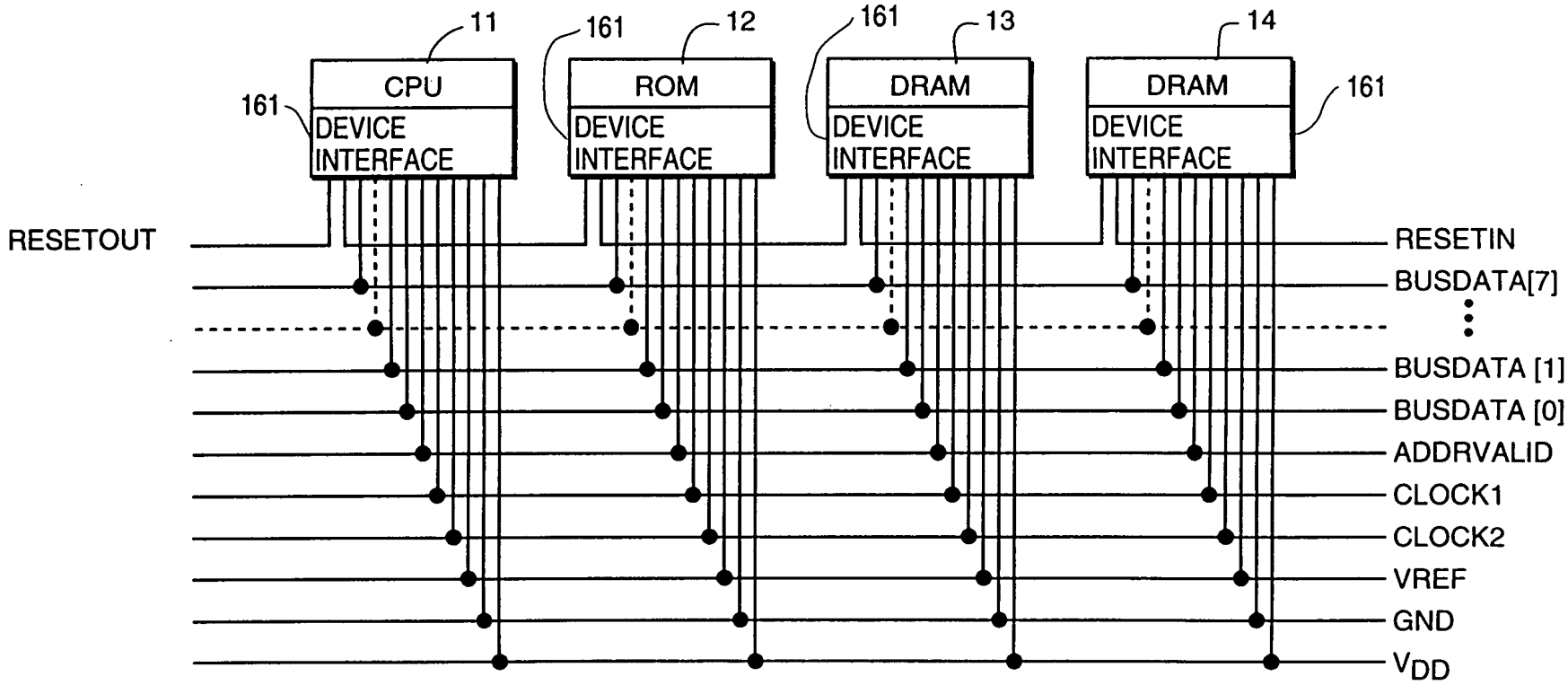
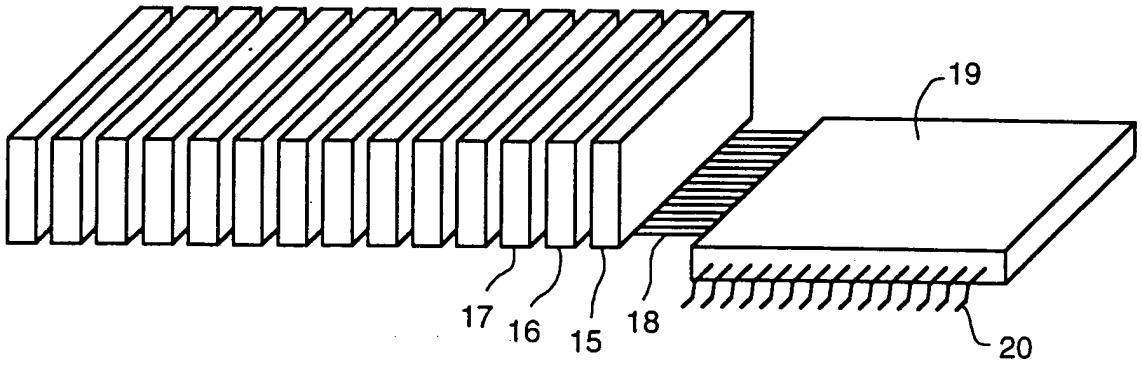

11
161
12
161
13
14
161
CPU
ROM
DRAM
DRAM
DEVICE INTERFACE
DEVICE INTERFACE
DEVICE INTERFACE
DEVICE INTERFACE
161
RESETOUT
RESETIN
BUSDATA[7]
BUSDATA [1]
BUSDATA [0]
ADDRVALID
CLOCK1
CLOCK2
VREF
GND
VDD

FIG_3



REGULAR ACCESS

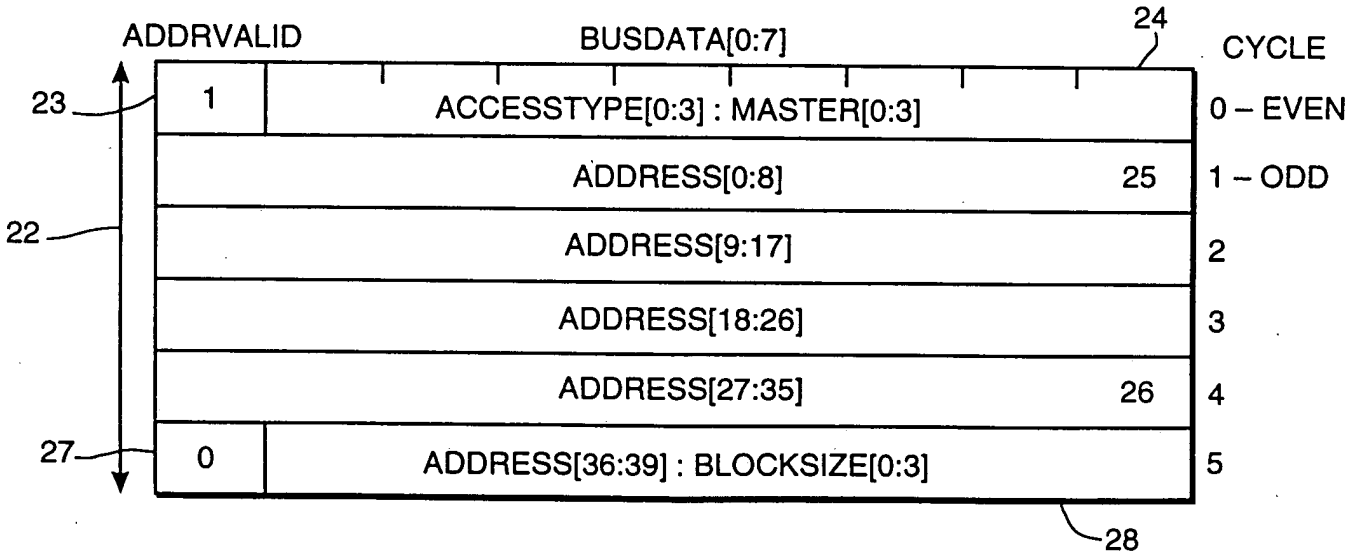


FIG_4

over

REJECT (NACK) CONTROL PACKET

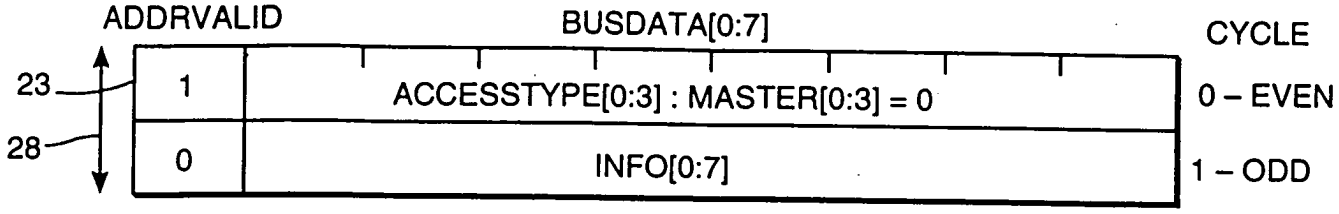


FIG_5

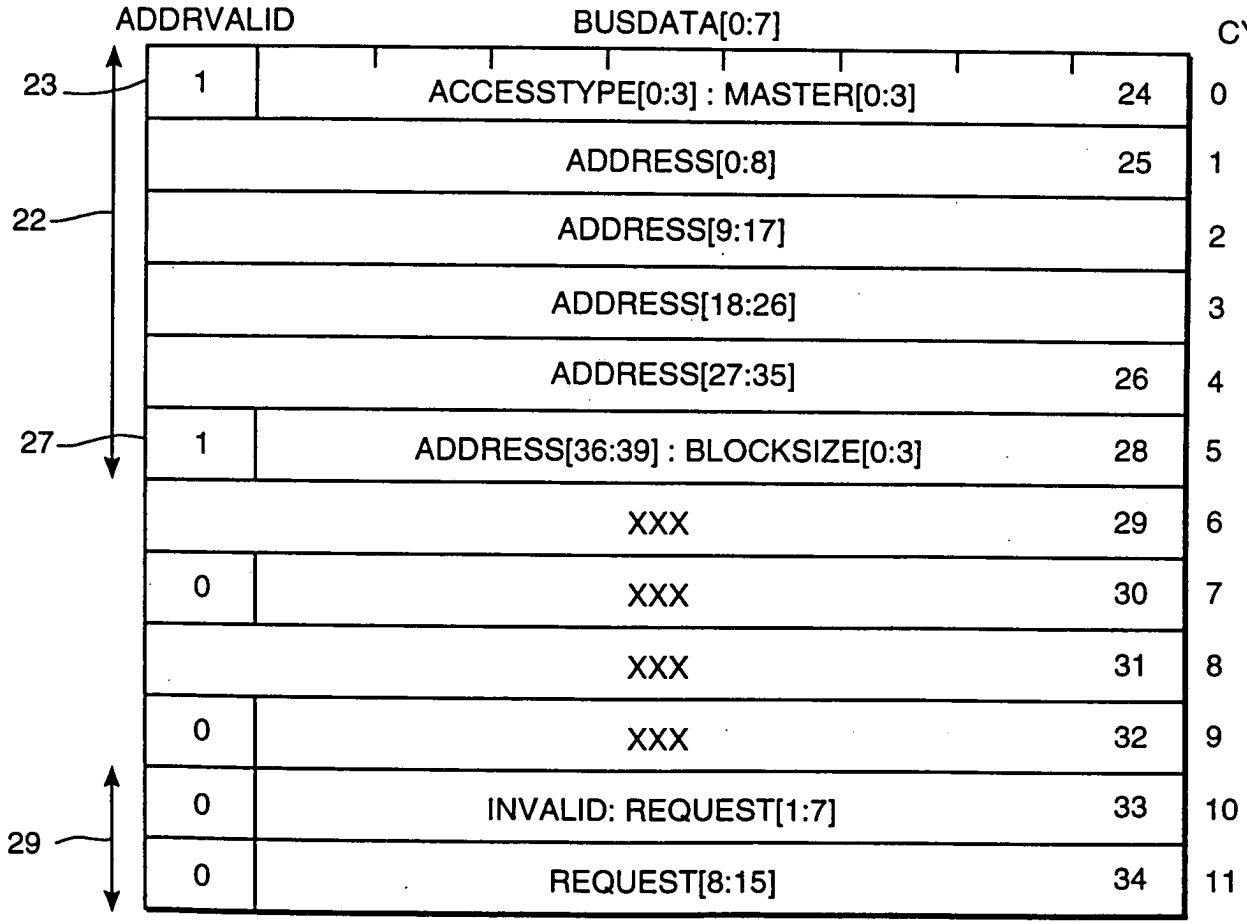


FIG_6

over

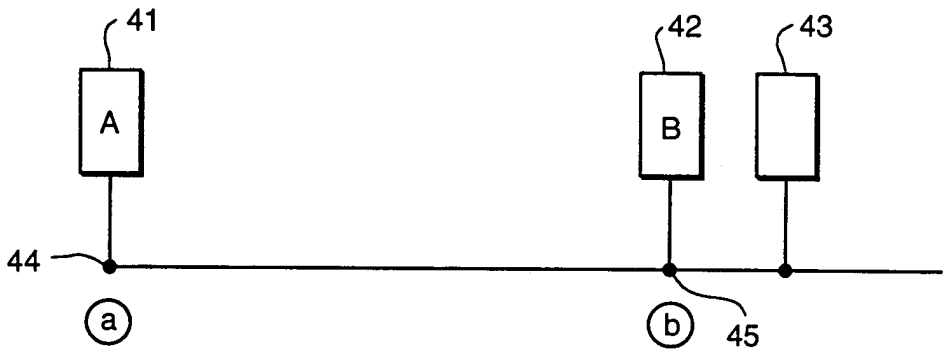


FIG_7A

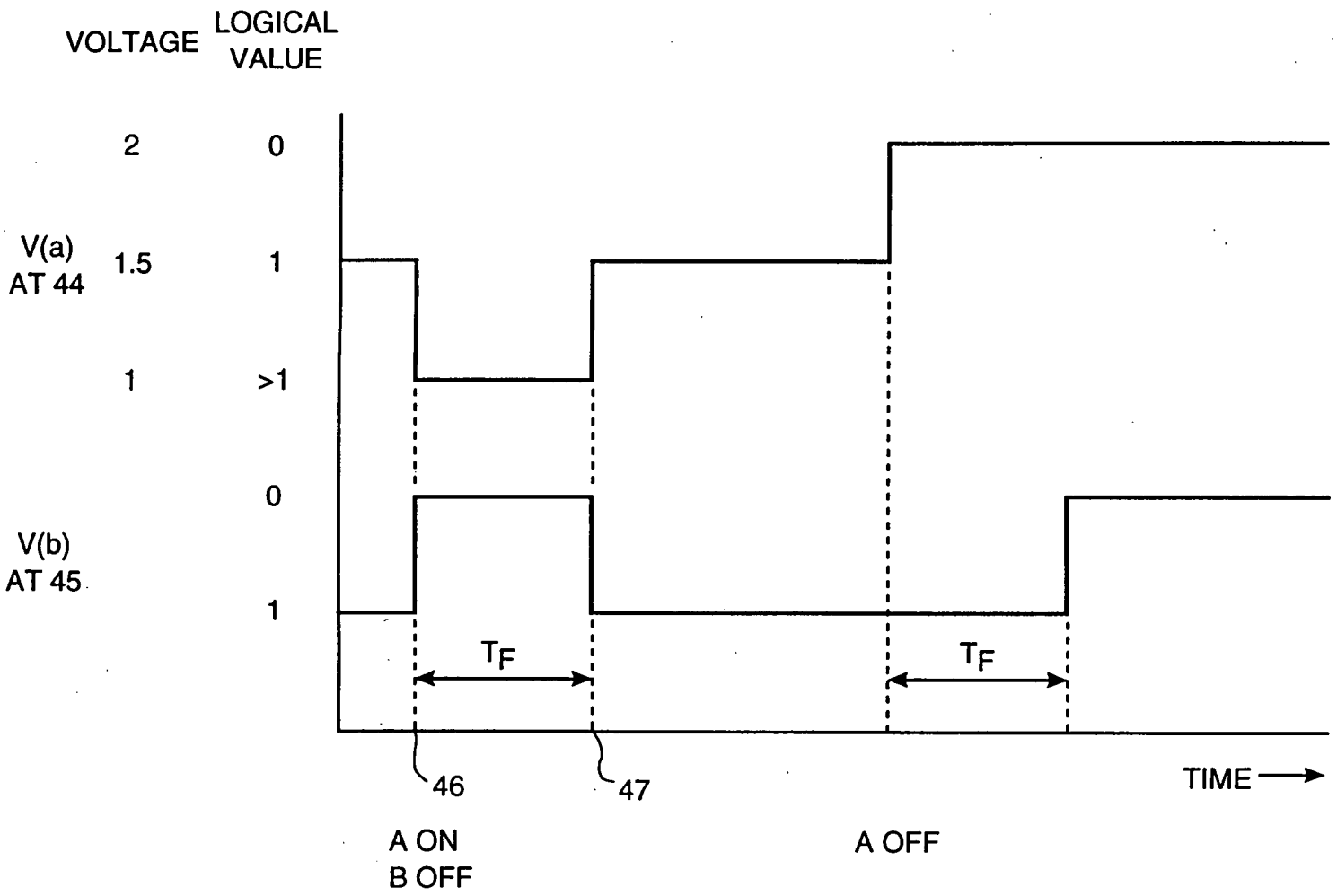

VOLTAGE
LOGICAL VALUE
2
0
V(a) AT 44
1.5
1
1
>1
0
V(b) AT 45
1
T_F
T_F
46
47
TIME
A ON
B OFF
A OFF

FIG_7B

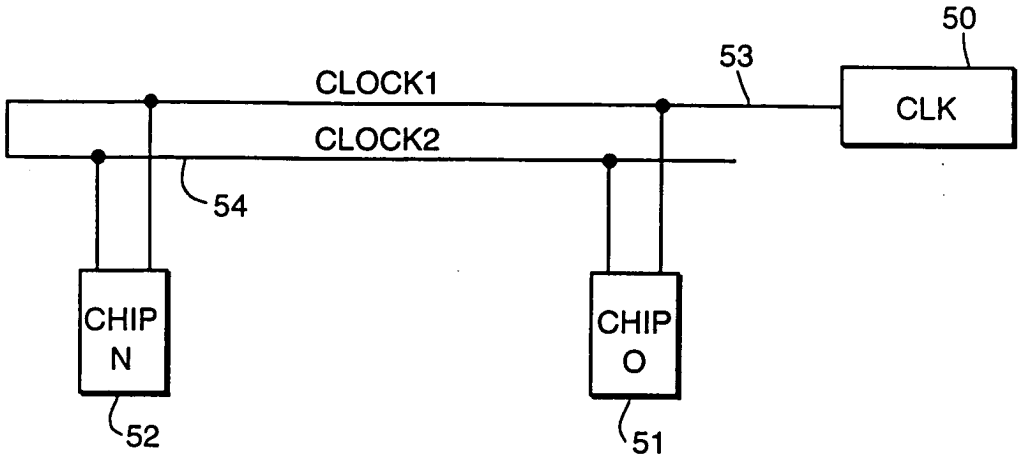

50
53
CLOCK1
CLK
CLOCK2
54
CHIP N
CHIP O
52
51

FIG_8A

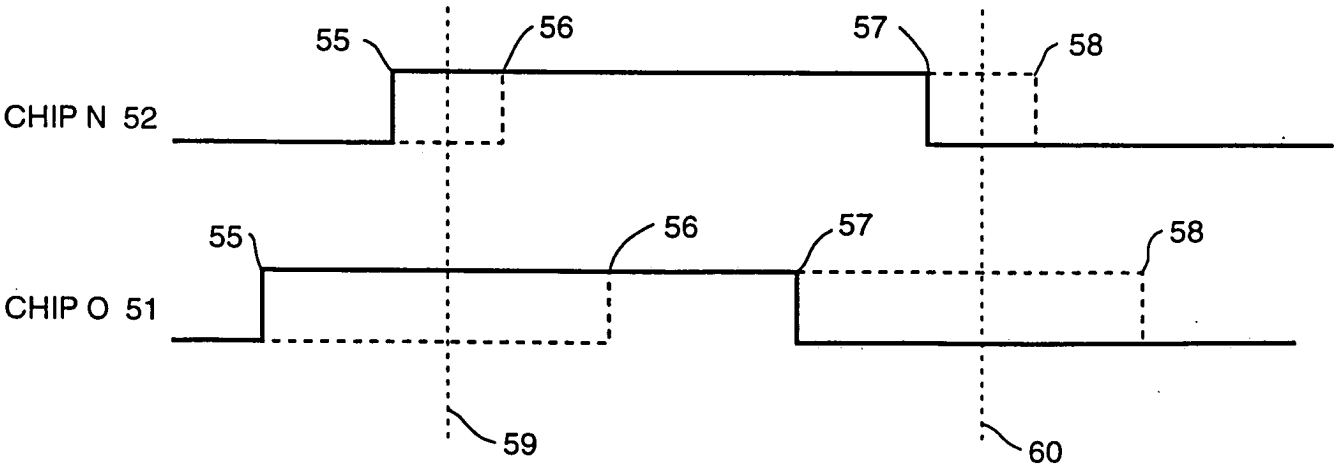

55
56
57
58
CHIP N 52
55
56
57
58
CHIP O 51
59
60

FIG_8B

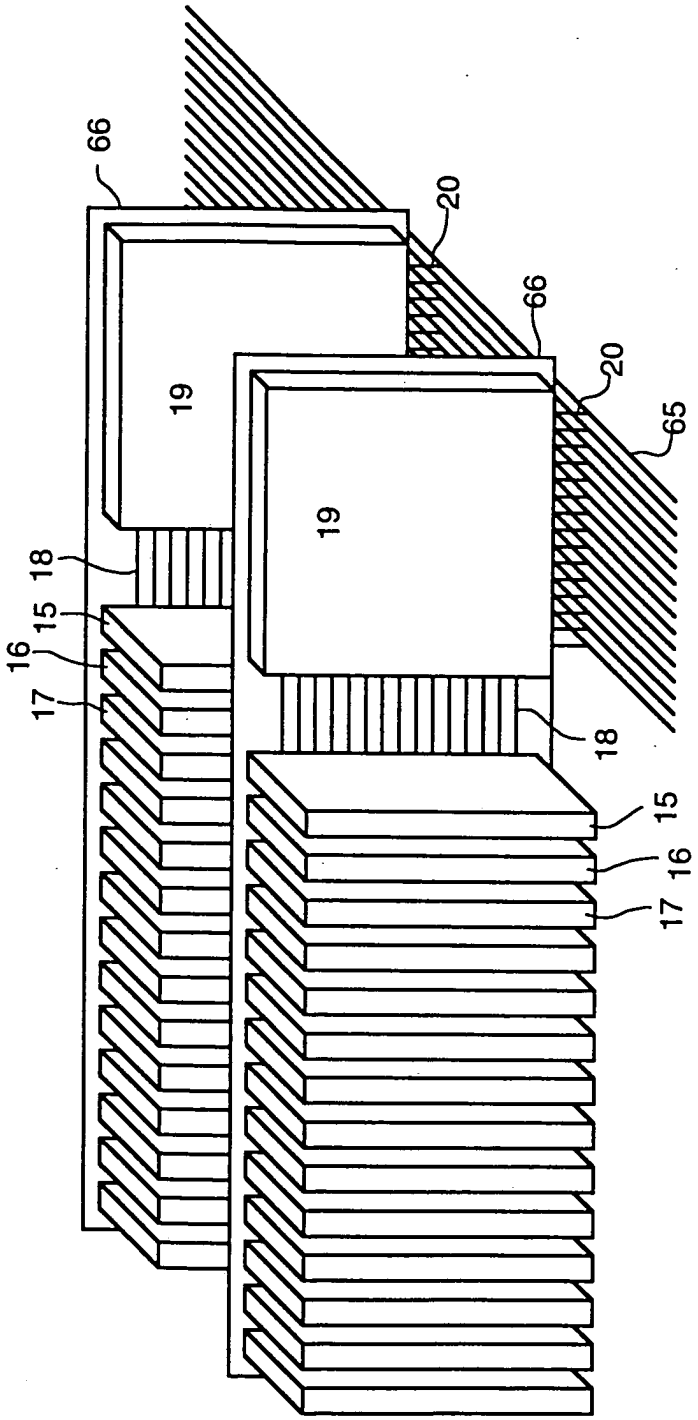


FIG_9

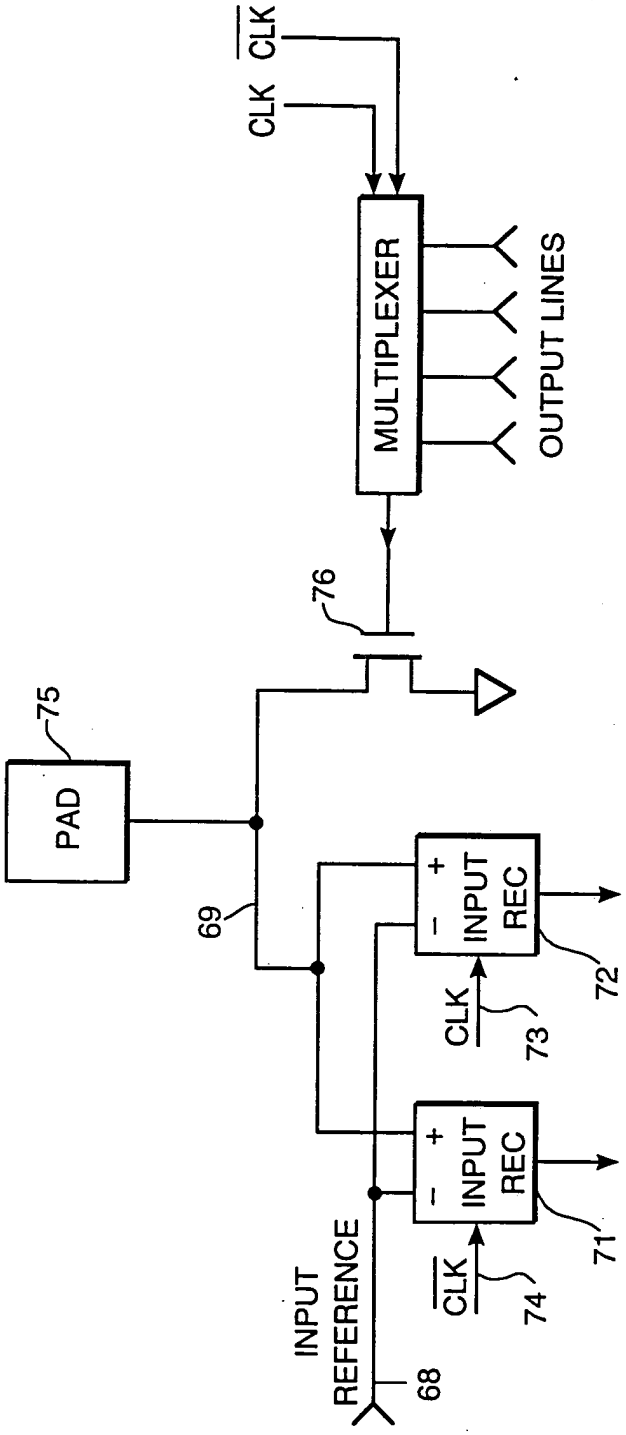

CLK
CLK
MULTIPLEXER
OUTPUT LINES
76
75
PAD
69
INPUT REC
72
CLK
73
INPUT REC
71
INPUT REFERENCE
68
CLK
74

FIG_ 10

over

FIG_11

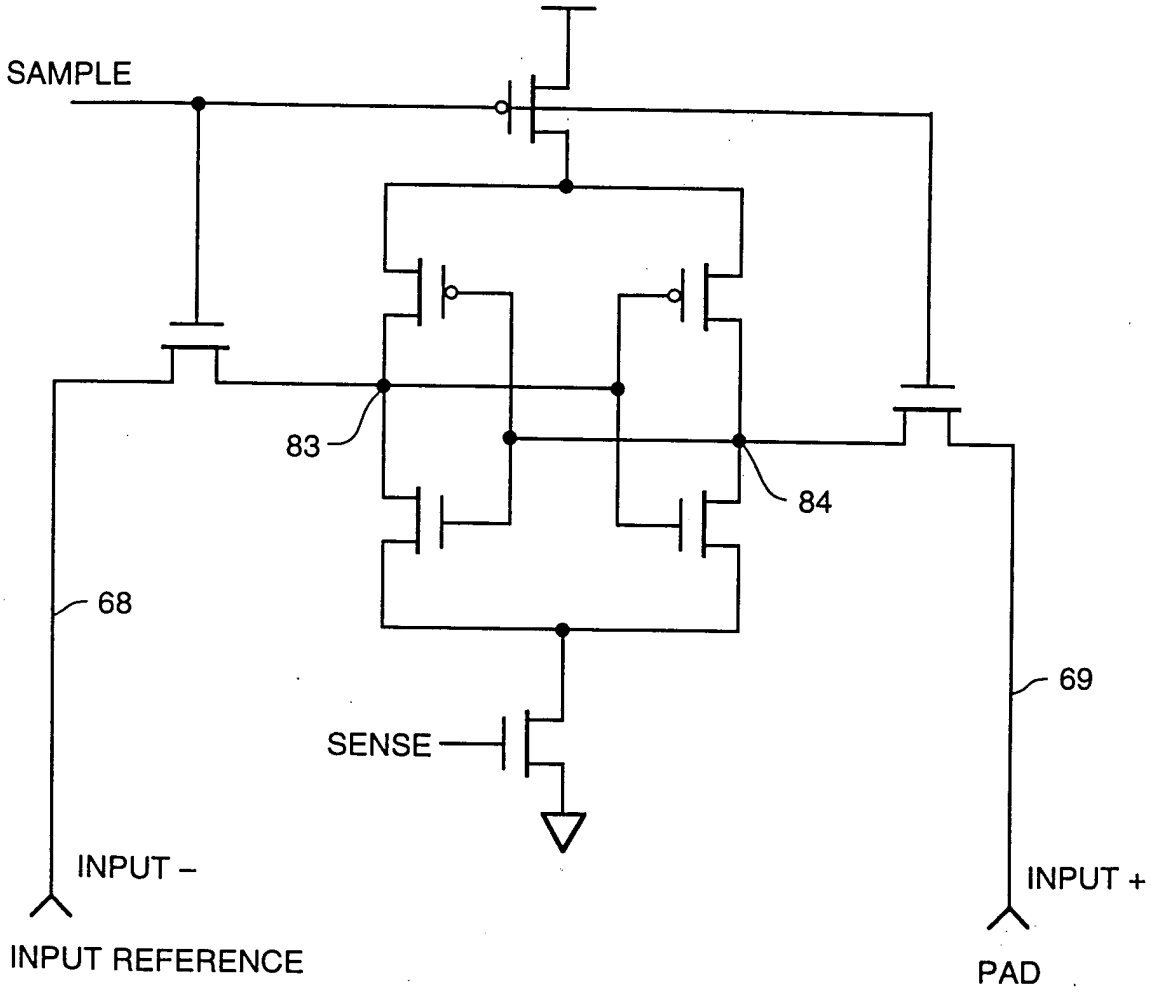


FIG_12

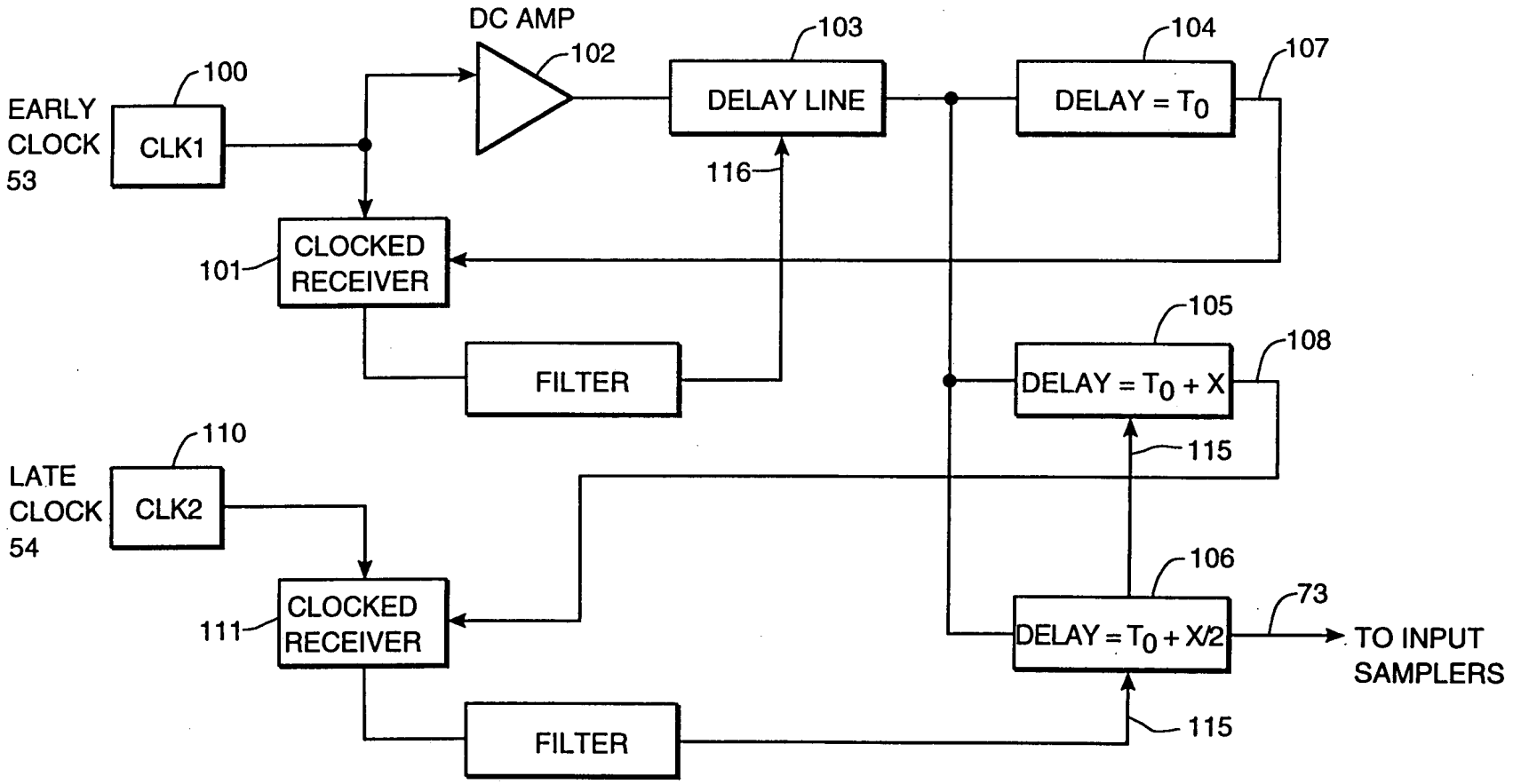
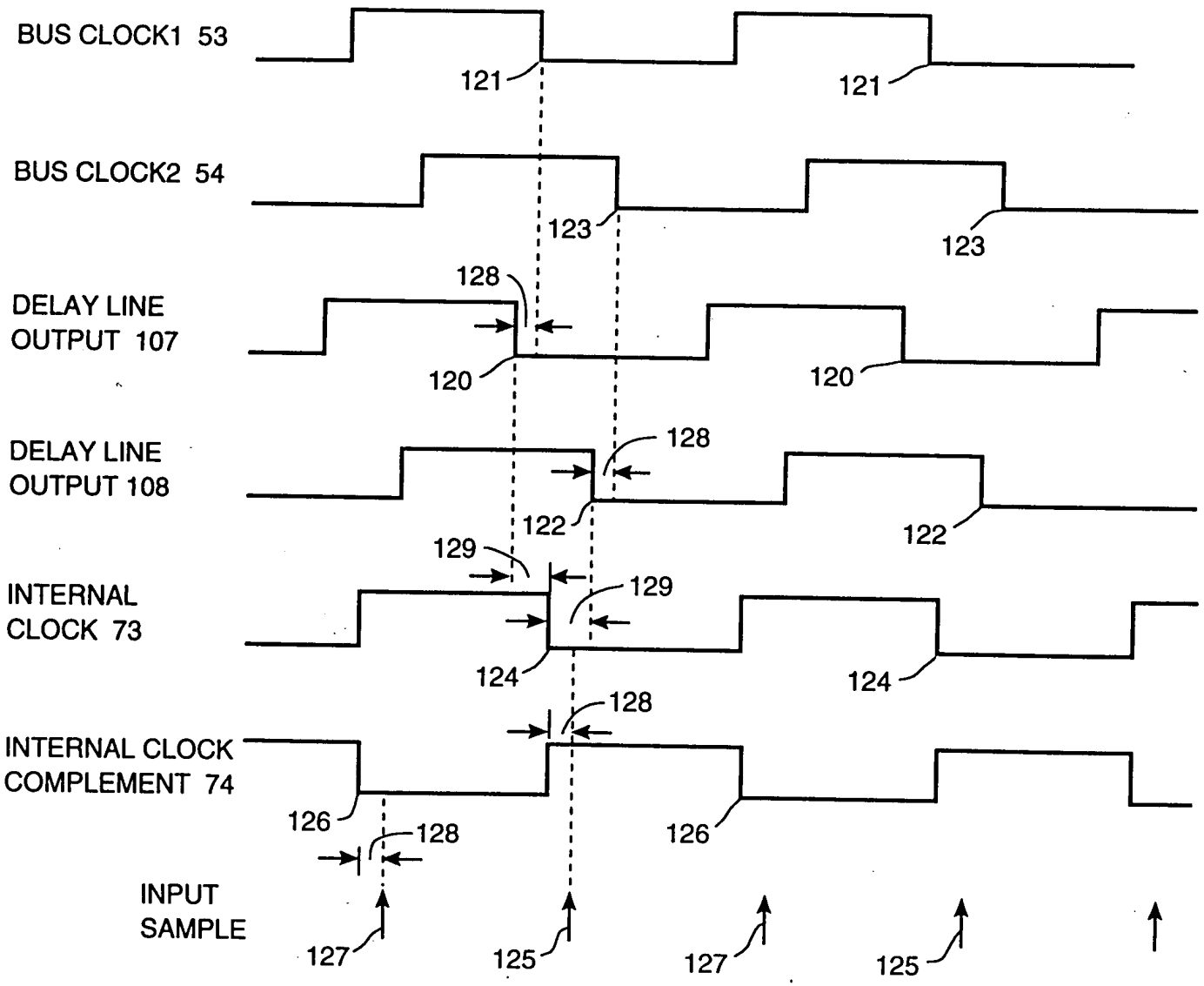

DC AMP
102
103
104
107
100
EARLY
CLOCK
53
CLK1
DELAY LINE
DELAY = T_0
116
101
CLOCKED
RECEIVER
105
108
FILTER
DELAY = T_0 + X
115
110
LATE
CLOCK
54
CLK2
106
73
CLOCKED
RECEIVER
111
DELAY = T_0 + X/2
TO INPUT
SAMPLERS
FILTER
115

FIG_13


BUS CLOCK1 53
121
121
BUS CLOCK2 54
123
123
DELAY LINE OUTPUT 107
128
120
120
DELAY LINE OUTPUT 108
128
122
122
INTERNAL CLOCK 73
129
129
124
124
INTERNAL CLOCK COMPLEMENT 74
128
126
126
128
INPUT SAMPLE
127
125
127
125

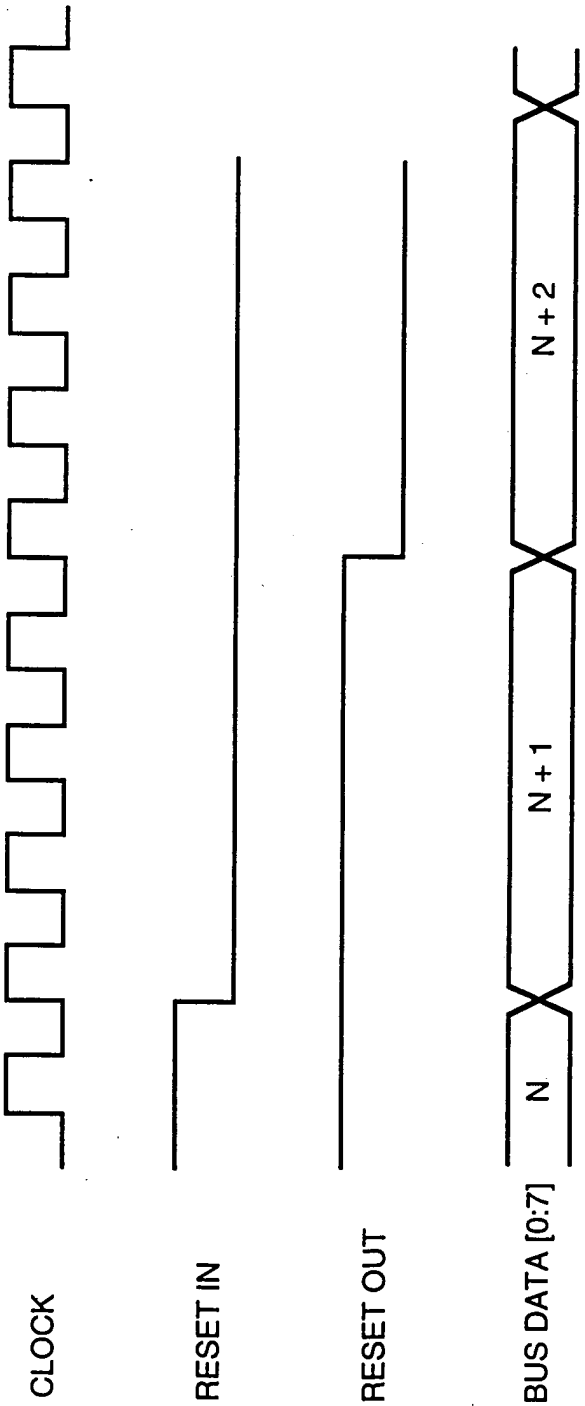
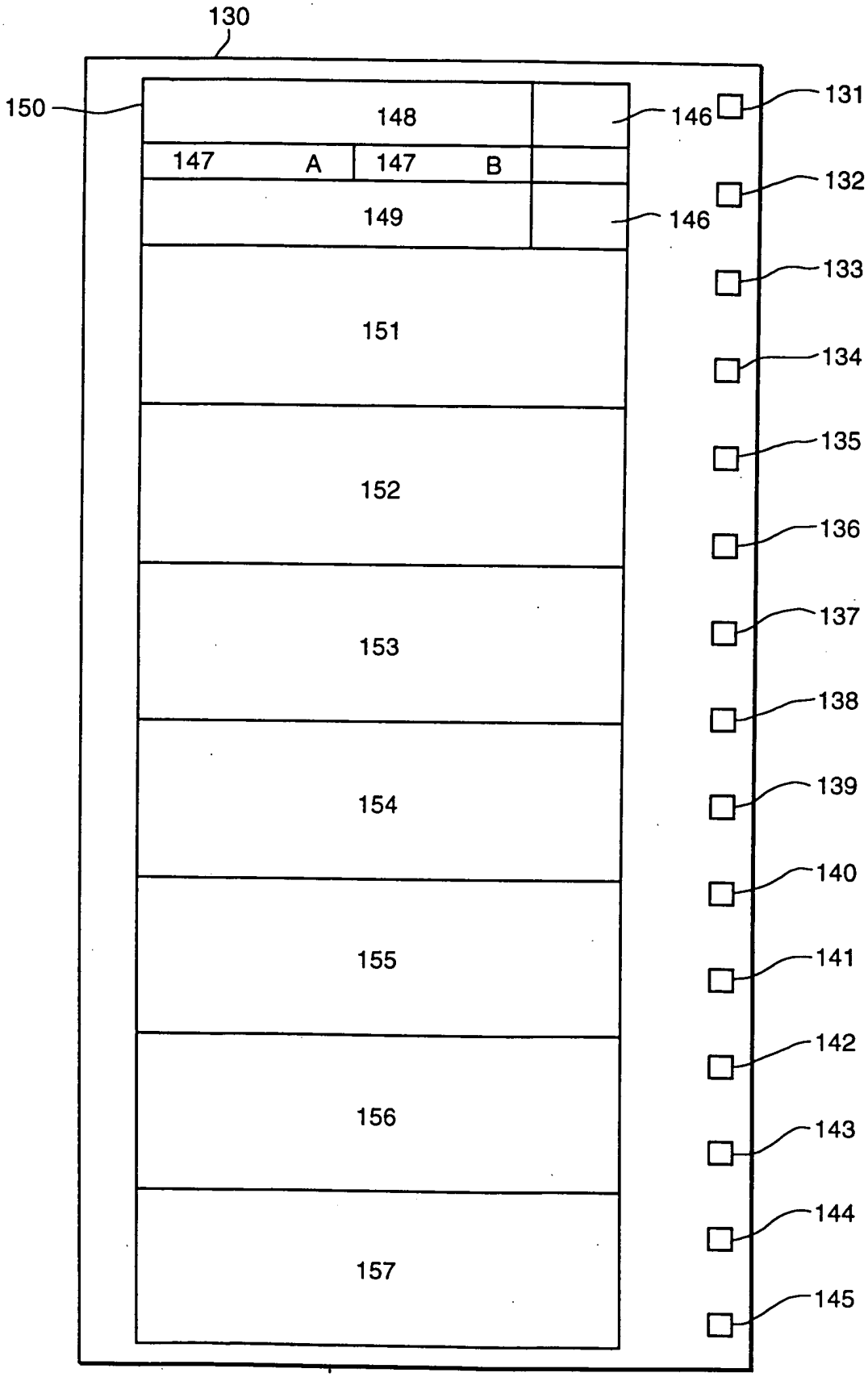


FIG_14

over

FIG_15


130
150
148
146
131
147 A
147 B
132
149
146
133
151
134
152
135
153
136
154
137
155
138
156
139
157
140
141
142
143
144
145

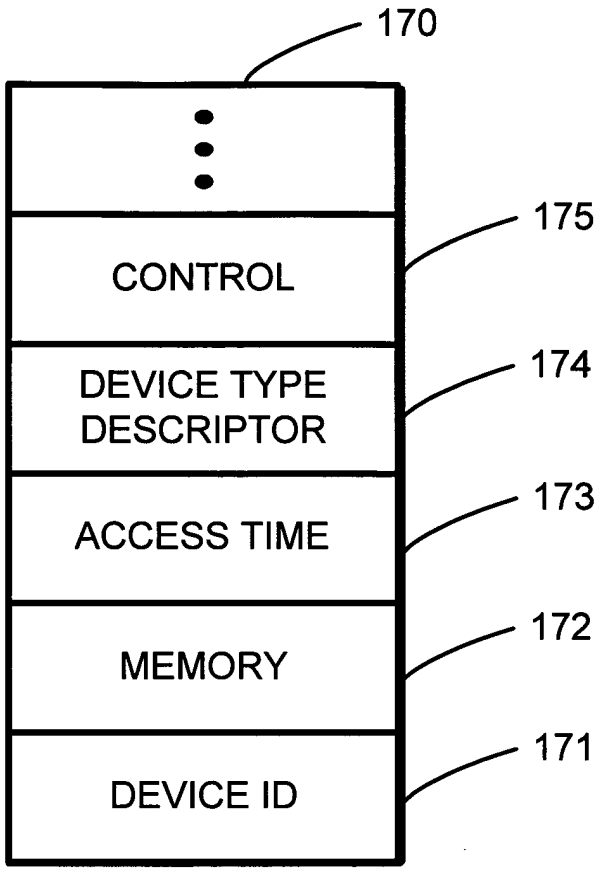

170
CONTROL
175
DEVICE TYPE DESCRIPTOR
174
ACCESS TIME
173
MEMORY
172
DEVICE ID
171

FIG. 16